

REMARKS

This is intended as a full and complete response to the Final Office Action dated May 23, 2007, having a shortened statutory period for response set to expire on August 23, 2007. Applicant submits this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1, 4-12, 14-20 and 22-24 are pending in the application. Claims 1, 4, 6-8, 10-12, 13-20 and 22-24 remain pending following entry of this response. Claims 1, 6-7, 10-11, 15 and 18 have been amended. Claims 5 and 9 have been cancelled. Applicant submits that the amendments and new claims do not introduce new matter.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 4-5, 7-10, 14-19 and 22-24 are rejected under 35 U.S.C. 102(b) as being fully anticipated by *Beffa et al.* (U.S. Patent No. 6,145,092, hereinafter, "*Beffa*").

Applicant respectfully traverses this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In this case, *Beffa* does not disclose "each and every element as set forth in the claim." For example, with respect to independent claims 1, 7, 15 and 18, *Beffa* does not disclose defect addresses that are stored in a memory unit which includes, for each word line group, a first memory segment having a first number of defect address memory locations for storing defect addresses in the respective word line group and, for each bit line group, a second memory segment having a second number of defect

address memory locations for storing defect addresses in the respective bit line group. The Examiner argues that *Beffa* discloses this element in Figure 2 (See 206 & 208). However, the cited passage is in fact directed to a row and column latch register that are simply “used to access data stored in [a] memory array.” (See col 4, lines 49-53). Nowhere is it mentioned that the latches are used to store defect addresses in a first or second memory segment of a memory unit.

Accordingly, Applicant submits that the cited reference does not disclose defect addresses that are stored in a memory unit which includes, for each word line group, a first memory segment having a first number of defect address memory locations for storing defect addresses in the respective word line group and, for each bit line group, a second memory segment having a second number of defect address memory locations for storing defect addresses in the respective bit line group. Therefore, withdrawal of the rejections for independent claims, 1, 7, 15 and 18 and the claims that depend therefrom are respectfully requested.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Claim Rejections - 35 U.S.C. § 103

Claims 6, 11-12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Beffa* and further in view of *Bemis* (U.S. Patent No. 4,692,894).

Claims 1, 7, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Tsutsumi et al.* (U.S. Patent No. 6,115,828, hereinafter, "*Tsutsumi*") and further in view of *Eaton et al.* (U.S. Patent No. 4,939,694, hereinafter, "*Eaton*"). The Examiner takes the position that it would have been obvious to one of the ordinary skill in the art at the time the invention was made to enable *Tsutsumi*'s invention with error correction and replacement capabilities of *Eaton*, because one of ordinary skill in the art would have realized that doing so will enable *Tsutsumi*'s invention to perform memory testing more efficiently.

Applicant respectfully traverses this rejection.

The Examiner's rejection of Claims 6, 11-12 and 20 incorporates the Examiner's rejection of corresponding claims 1, 7, 15 and 18 in view of *Beffa*. As stated earlier, the rejection of independent Claims 1, 7, 15 and 18 in view of *Beffa* is believed to be overcome. Accordingly, the rejection of Claims 6, 11-12 and 20 is also believed to be overcome. Therefore, withdrawal of the rejection is respectfully requested.

In regards to Examiner's rejection of independent claims 1, 7, 15 and 18 in view of *Tsutsumi* and in further view of *Eaton*, these claims have been amended to include the limitations of claim 5. The limitations of claim 5 were not rejected under 35 U.S.C. 103(a). Furthermore, neither *Tsutsumi* nor *Eaton* teach the limitations of amended independent claims 1, 7, 15 and 18. Specifically, *Tsutsumi* and *Eaton* do not disclose defect addresses that are stored in a memory unit which includes, for each word line group, a first memory segment having a first number of defect address memory locations for storing defect addresses in the respective word line group and, for each bit line group, a second memory segment having a second number of defect address memory locations for storing defect addresses in the respective bit line group.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

If the Examiner believes any issues remain that prevent this application from going to issue, the Examiner is strongly encouraged to contact the undersigned attorney to discuss strategies for moving prosecution forward toward allowance.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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